

IN THE SPECIFICATION:

Please replace paragraph number [0044] with the following rewritten paragraph:

[0044] With continued reference to FIG. 4, the resulting chip-scale package 40 includes a semiconductor device component 12 and a substantially defect-free protective layer 20 secured to at least a portion of the upper or active surface 13 of semiconductor device component 12. A conductive structure 18, which is secured to and in electrical communication with a contact pad 16 of semiconductor device component 12, may protrude through protective layer 20. When chip-scale package 40 includes one or more protruding conductive structures 18, support structures 22', which result from the formation of a meniscus 22 around base portion 19 of each conductive structure 18, may substantially surround base portion 19 and provide mechanical support for the same. An edge cover 26 of chip-scale package 40 may substantially cover the junction between peripheral edges 15 of semiconductor device component 12 and upper or active surface 13 thereof, preventing delamination of protective layer 20 therefrom, as well as at least partially protecting peripheral edges 15.

Please replace paragraph number [0046] with the following rewritten paragraph:

[0046] In FIG. 5, a fabrication substrate 10 is depicted as including a plurality of yet-to-be singulated semiconductor device components 12, a street 14 between semiconductor device components 12, conductive structures 18 secured to and protruding from contact pads 16 on upper or active surfaces 13 of semiconductor device components 12, and a protective layer 20 formed on upper or active surfaces 13. Protective layer 20 forms a meniscus 22 around and substantially surrounding a base portion 19 of each conductive structure 18. Protective layer 20 may be applied to upper or active surface 13 of each semiconductor device component 12 as described above in reference to FIG. 2.